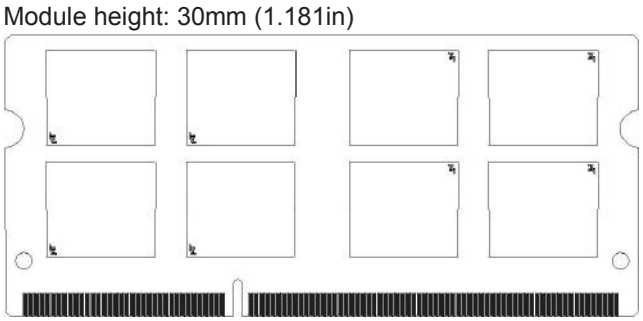
1.35V DDR3L SDRAM SODIMM

NTCKF1600ND3-4GB
NTCKF1600ND3-8GB

Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 204-pin, small outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3-14900, PC3-12800, or PC3-10600
- 4GB , 8GB
- V_{DD} = 1.35V (1.283V–1.45V)
- V_{DDSPD} = 3.0–3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- On-board I^2C serial presence-detect (SPD) EEPROM
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 204-Pin SODIMM (MO-268 R/C-F, R/C-F3)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ TA ≤ +70°C)	None
• Package	
– 204-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.07ns @ CL = 13 (DDR3-1866)	-1G9
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4

Pin Assignments

Table 5: Pin Assignments

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	DQ19	105	V_{DD}	157	DQ42	2	V_{SS}	54	V_{SS}	106	V_{DD}	158	DQ46
3	V_{SS}	55	V_{SS}	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	V_{SS}	6	DQ5	58	DQ29	110	RAS#	162	V_{SS}
7	DQ1	59	DQ25	111	V_{DD}	163	DQ48	8	V_{SS}	60	V_{SS}	112	V_{DD}	164	DQ52
9	V_{SS}	61	V_{SS}	113	WE#	165	DQ49	10	DQS0#	62	DQS3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	V_{SS}	12	DQS0	64	DQS3	116	ODT0	168	V_{SS}
13	V_{SS}	65	V_{SS}	117	V_{DD}	169	DQS6#	14	V_{SS}	66	V_{SS}	118	V_{DD}	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	ODT1	172	V_{SS}
17	DQ3	69	DQ27	121	S1#	173	V_{SS}	18	DQ7	70	DQ31	122	NC	174	DQ54
19	V_{SS}	71	V_{SS}	123	V_{DD}	175	DQ50	20	V_{SS}	72	V_{SS}	124	V_{DD}	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	CKE1	126	V_{REFCA}	178	V_{SS}
23	DQ9	75	V_{DD}	127	V_{SS}	179	V_{SS}	24	DQ13	76	V_{DD}	128	V_{SS}	180	DQ60
25	V_{SS}	77	NC	129	DQ32	181	DQ56	26	V_{SS}	78	NC/A15[1]	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80	A14	132	DQ37	184	V_{SS}
29	DQS1	81	V_{DD}	133	V_{SS}	185	V_{SS}	30	RESET#	82	V_{DD}	134	V_{SS}	186	DQS7#
31	V_{SS}	83	A12	135	DQS4#	187	DM7	32	V_{SS}	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	V_{SS}	34	DQ14	86	A7	138	V_{SS}	190	V_{SS}
35	DQ11	87	V_{DD}	139	V_{SS}	191	DQ58	36	DQ15	88	V_{DD}	140	DQ38	192	DQ62
37	V_{SS}	89	A8	141	DQ34	193	DQ59	38	V_{SS}	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	V_{SS}	40	DQ20	92	A4	144	V_{SS}	196	V_{SS}
41	DQ17	93	V_{DD}	145	V_{SS}	197	SA0	42	DQ21	94	V_{DD}	146	DQ44	198	NF
43	V_{SS}	95	A3	147	DQ40	199	V_{DDSPD}	44	V_{SS}	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	V_{SS}	202	SCL
47	DQS2	99	V_{DD}	151	V_{SS}	203	V_{TT}	48	V_{SS}	100	V_{DD}	152	DQS5#	204	V_{TT}
49	V_{SS}	101	CK0	153	DM5	–	–	50	DQ22	102	CK1	154	DQS5	–	–
51	DQ18	103	CK0#	155	V_{SS}	–	–	52	DQ23	104	CK1#	156	V_{SS}	–	–

Note: 1. Pin 78 is NC 4GB, A15 for 8GB.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 6: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

DQ Map

Table 7: Component-to-Module DQ Map, PCB 0900 R/C-F (Front)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	15	U2	0	18	51
	1	5	6		1	21	42
	2	3	17		2	19	53
	3	0	5		3	16	39
	4	6	16		4	22	50
	5	4	4		5	20	40
	6	7	18		6	23	52
	7	1	7		7	17	41
U5	0	42	157	U6	0	58	191
	1	45	148		1	61	182
	2	43	159		2	59	193
	3	40	147		3	56	181
	4	46	158		4	62	192
	5	44	146		5	60	180
	6	47	160		6	63	194
	7	41	149		7	57	183
U7	0	13	24	U8	0	26	67
	1	10	33		1	29	58
	2	8	21		2	27	69
	3	11	35		3	24	57
	4	9	23		4	30	68
	5	15	36		5	28	56
	6	12	22		6	31	70
	7	14	34		7	25	59
U9	0	34	141	U10	0	53	166
	1	37	132		1	50	175
	2	35	143		2	48	163
	3	32	129		3	51	177
	4	38	140		4	49	165
	5	36	130		5	55	176
	6	39	142		6	52	164
	7	33	131		7	54	174

Table 8: Component-to-Module DQ Map, PCB 0900 R/C-F (Back)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	61	182	U12	0	45	148
	1	58	191		1	42	157
	2	56	181		2	40	147
	3	59	193		3	43	159
	4	57	183		4	41	149
	5	63	194		5	47	160
	6	60	180		6	44	146
	7	62	192		7	46	158
U15	0	21	42	U16	0	5	6
	1	18	51		1	2	15
	2	16	39		2	0	5
	3	19	53		3	3	17
	4	17	41		4	1	7
	5	23	52		5	7	18
	6	20	40		6	4	4
	7	22	50		7	6	16
U17	0	50	175	U18	0	37	132
	1	53	166		1	34	141
	2	51	177		2	32	129
	3	48	163		3	35	143
	4	54	174		4	33	131
	5	52	164		5	39	142
	6	55	176		6	36	130
	7	49	165		7	38	140
U19	0	29	58	U20	0	10	33
	1	26	67		1	13	24
	2	24	57		2	11	35
	3	27	69		3	8	21
	4	25	59		4	14	34
	5	31	70		5	12	22
	6	28	56		6	15	36
	7	30	68		7	9	23

Table 9: Component-to-Module DQ Map, PCB 1569 R/C-F3 (Front)

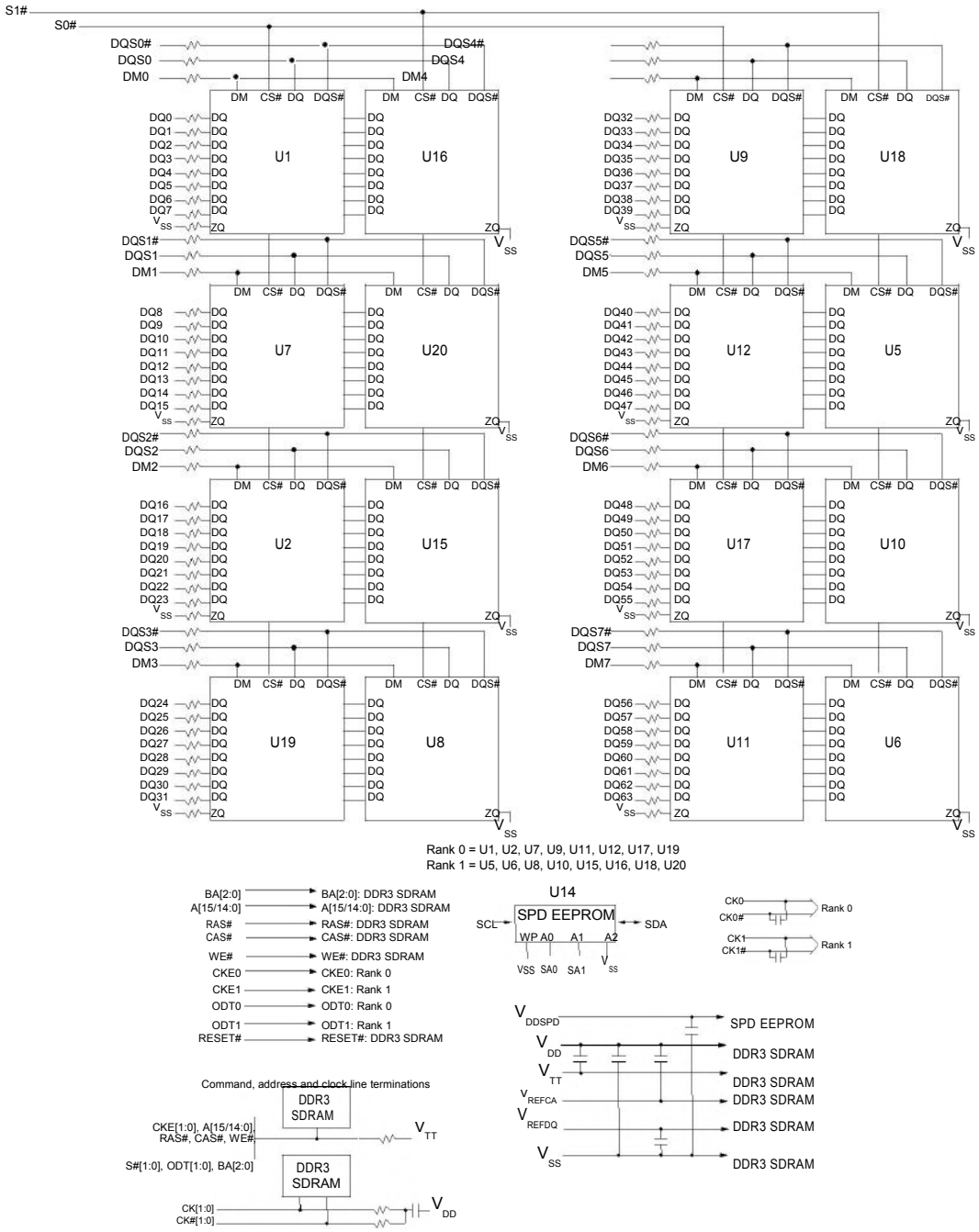
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	2	13	U3	0	18	49
	1	5	6		1	21	42
	2	3	15		2	19	51
	3	0	5		3	16	37
	4	6	16		4	22	48
	5	4	4		5	20	40
	6	7	18		6	23	50
	7	1	7		7	17	39
U4	0	42	159	U5	0	58	191
	1	45	150		1	61	182
	2	43	161		2	59	193
	3	40	151		3	56	183
	4	46	160		4	62	192
	5	44	148		5	60	180
	6	47	162		6	63	194
	7	41	153		7	57	185
U6	0	13	24	U7	0	26	63
	1	10	31		1	29	56
	2	8	19		2	27	65
	3	11	33		3	24	55
	4	9	21		4	30	66
	5	15	36		5	28	54
	6	12	22		6	31	68
	7	14	34		7	25	57
U8	0	34	145	U9	0	53	168
	1	37	136		1	50	177
	2	35	147		2	48	165
	3	32	133		3	51	179
	4	38	142		4	49	167
	5	36	134		5	55	176
	6	39	144		6	52	166
	7	33	135		7	54	174

Table 10: Component-to-Module DQ Map, PCB 1569 R/C-F (Back)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	61	182	U12	0	45	150
	1	58	191		1	42	159
	2	56	183		2	40	151
	3	59	193		3	43	161
	4	57	185		4	41	153
	5	63	194		5	47	162
	6	60	180		6	44	148
	7	62	192		7	46	160
U13	0	21	42	U14	0	5	6
	1	18	49		1	2	13
	2	16	37		2	0	5
	3	19	51		3	3	15
	4	17	39		4	1	7
	5	23	50		5	7	18
	6	20	40		6	4	4
	7	22	48		7	6	16
U15	0	50	177	U16	0	37	136
	1	53	168		1	34	145
	2	51	179		2	32	133
	3	48	165		3	35	147
	4	54	174		4	33	135
	5	52	166		5	39	144
	6	55	176		6	36	134
	7	49	167		7	38	142
U17	0	29	56	U18	0	10	31
	1	26	63		1	13	24
	2	24	55		2	11	33
	3	27	65		3	8	19
	4	25	57		4	14	34
	5	31	68		5	12	22
	6	28	54		6	15	36
	7	30	66		7	9	21

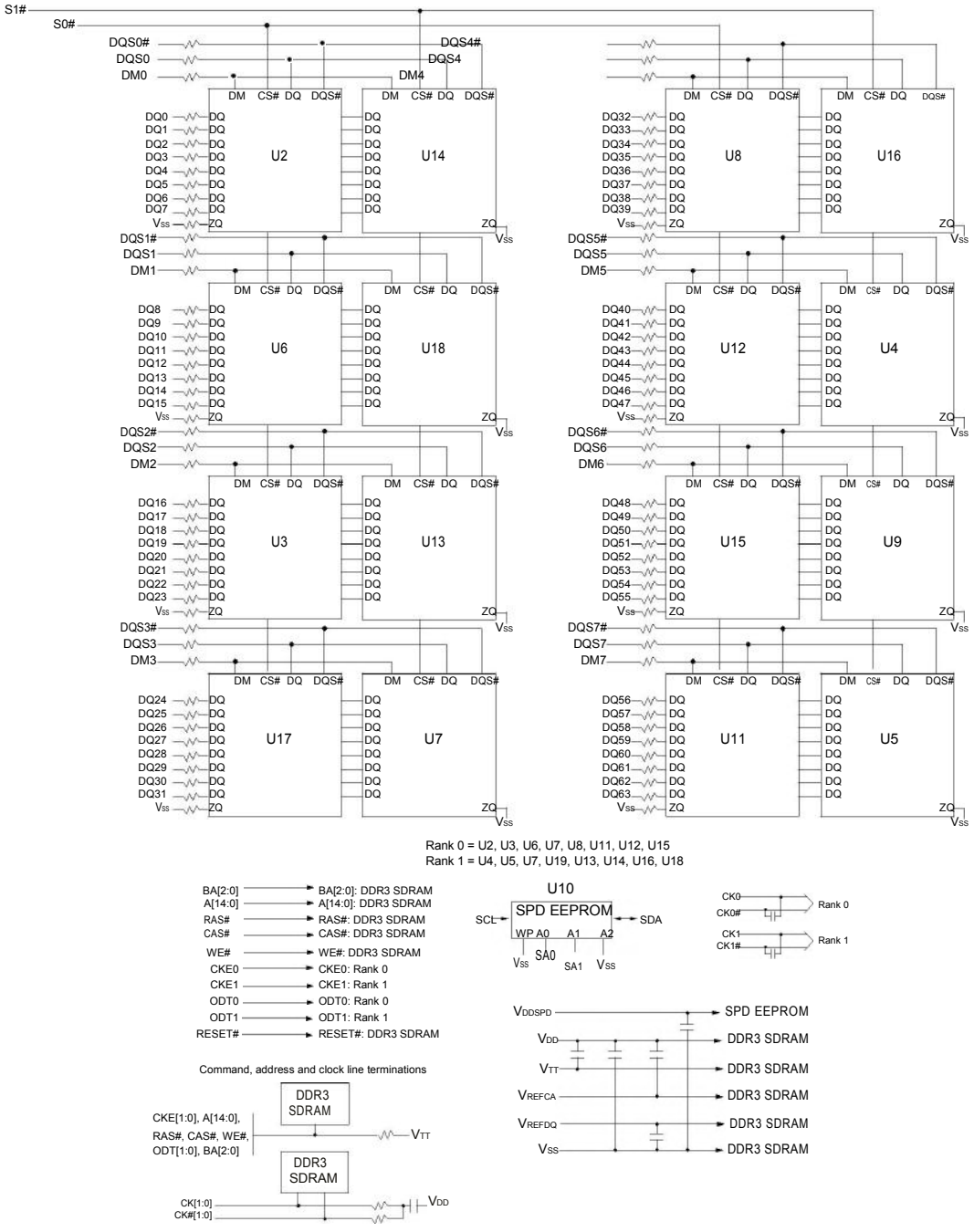
Functional Block Diagram

Figure 2: Functional Block Diagram (PCB 0900, R/C-F)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Figure 3: Functional Block Diagram (PCB 1569, R/C-F3)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory mod-ules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM mod-ules use DDR architecture to achieve high-speed operation. DDR3 architecture is essen-tially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM mod-ule effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the inter-nal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, com-mand, and address buses have been routed in a fly-by topology, where each clock, con-trol, command, and address pin on each DRAM is connected to a single trace and ter-minated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS sig-nals can be easily accounted for by using the write-leveling feature of DDR3.

I_{DD} Specifications

Table 14: DDR3 I_{DD} Specifications and Conditions – 4GB (Die Revision K)

Values are for the MT41K256M8 DDR3L SDRAM only and are computed from values specified in the 1.35V 2Gb component data sheet

Parameter	Symbol	1600	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	408	400	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	512	496	mA
Precharge power-down current: Slow exit	I_{DD2P0}[2]	192	192	mA
Precharge power-down current: Fast exit	I_{DD2P1}[2]	224	224	mA
Precharge quiet standby current	I_{DD2Q}[2]	320	320	mA
Precharge standby current	I_{DD2N}[2]	336	336	mA
Precharge standby ODT current	I_{DD2NT}[1]	344	328	mA
Active power-down current	I_{DD3P}[2]	336	336	mA
Active standby current	I_{DD3N}[2]	512	480	mA
Burst read operating current	I_{DD4R}[1]	848	752	mA
Burst write operating current	I_{DD4W}[1]	872	776	mA
Refresh current	I_{DD5B}[1]	1536	1528	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	192	192	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	240	240	mA
All banks interleaved read current	I_{DD7}[1]	1344	1296	mA
Reset current	I_{DD8}[2]	224	224	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit). 2. All ranks in this I_{DD} condition.

Table 15: DDR3 I_{DD} Specifications and Conditions – 8GB (Die Revisions E)

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb component data sheet

Parameter	Symbol	1866	1600	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	640	584	520	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	704	672	640	mA
Precharge power-down current: Slow exit	I_{DD2P0}[2]	288	288	288	mA
Precharge power-down current: Fast exit	I_{DD2P1}[2]	592	512	448	mA
Precharge quiet standby current	I_{DD2Q}[2]	560	512	448	mA
Precharge standby current	I_{DD2N}[2]	560	512	464	mA
Precharge standby ODT current	I_{DD2NT}[1]	480	456	424	mA
Active power-down current	I_{DD3P}[2]	656	608	560	mA
Active standby current	I_{DD3N}[2]	656	608	560	mA
Burst read operating current	I_{DD4R}[1]	1536	1400	1264	mA
Burst write operating current	I_{DD4W}[1]	1272	1144	1024	mA
Refresh current	I_{DD5B}[1]	2080	2024	1968	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	320	320	320	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	400	400	400	mA
All banks interleaved read current	I_{DD7}[1]	2152	1904	1664	mA
Reset current	I_{DD8}[2]	320	320	320	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit). 2. All ranks in this I_{DD} condition.

Table 16: DDR3 I_{DD} Specifications and Conditions – 8GB (Die Revision N)

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb component data sheet

Parameter	Symbol	1866	1600	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	456	440	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	576	552	mA
Precharge power-down current: Slow exit	I_{DD2P0}[2]	128	128	mA
Precharge power-down current: Fast exit	I_{DD2P1}[2]	256	224	mA
Precharge quiet standby current	I_{DD2Q}[2]	416	384	mA
Precharge standby current	I_{DD2N}[2]	416	384	mA
Precharge standby ODT current	I_{DD2NT}[1]	304	288	mA
Active power-down current	I_{DD3P}[2]	448	416	mA
Active standby current	I_{DD3N}[2]	512	480	mA
Burst read operating current	I_{DD4R}[1]	904	824	mA
Burst write operating current	I_{DD4W}[1]	904	824	mA
Refresh current	I_{DD5B}[1]	1504	1464	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	192	192	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	256	256	mA
All banks interleaved read current	I_{DD7}[1]	1184	1104	mA
Reset current	I_{DD8}[2]	160	160	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit). 2. All ranks in this I_{DD} condition.

Table 17: DDR3 I_{DD} Specifications and Conditions – 8GB (Die Revision P)

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb component data sheet

Parameter	Symbol	1866	1600	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	320	304	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	440	424	mA
Precharge power-down current: Slow exit	I_{DD2P0}[2]	176	160	mA
Precharge power-down current: Fast exit	I_{DD2P1}[2]	176	176	mA
Precharge quiet standby current	I_{DD2Q}[2]	240	240	mA
Precharge standby current	I_{DD2N}[2]	272	256	mA
Precharge standby ODT current	I_{DD2NT}[1]	264	240	mA
Active power-down current	I_{DD3P}[2]	240	240	mA
Active standby current	I_{DD3N}[2]	336	320	mA
Burst read operating current	I_{DD4R}[1]	904	800	mA
Burst write operating current	I_{DD4W}[1]	992	888	mA
Refresh current	I_{DD5B}[1]	1304	1296	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	240	240	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	368	368	mA
All banks interleaved read current	I_{DD7}[1]	1256	1120	mA
Reset current	I_{DD8}[2]	208	208	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P0} (slow exit). 2. All ranks in this I_{DD} condition.

Serial Presence-Detect EEPROM

For the latest SPD data, refer to Micron's SPD page: micron.com/spd.

Table 18: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.45	V_{DDSPD} x 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 1.0	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	2.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	2.0	µA

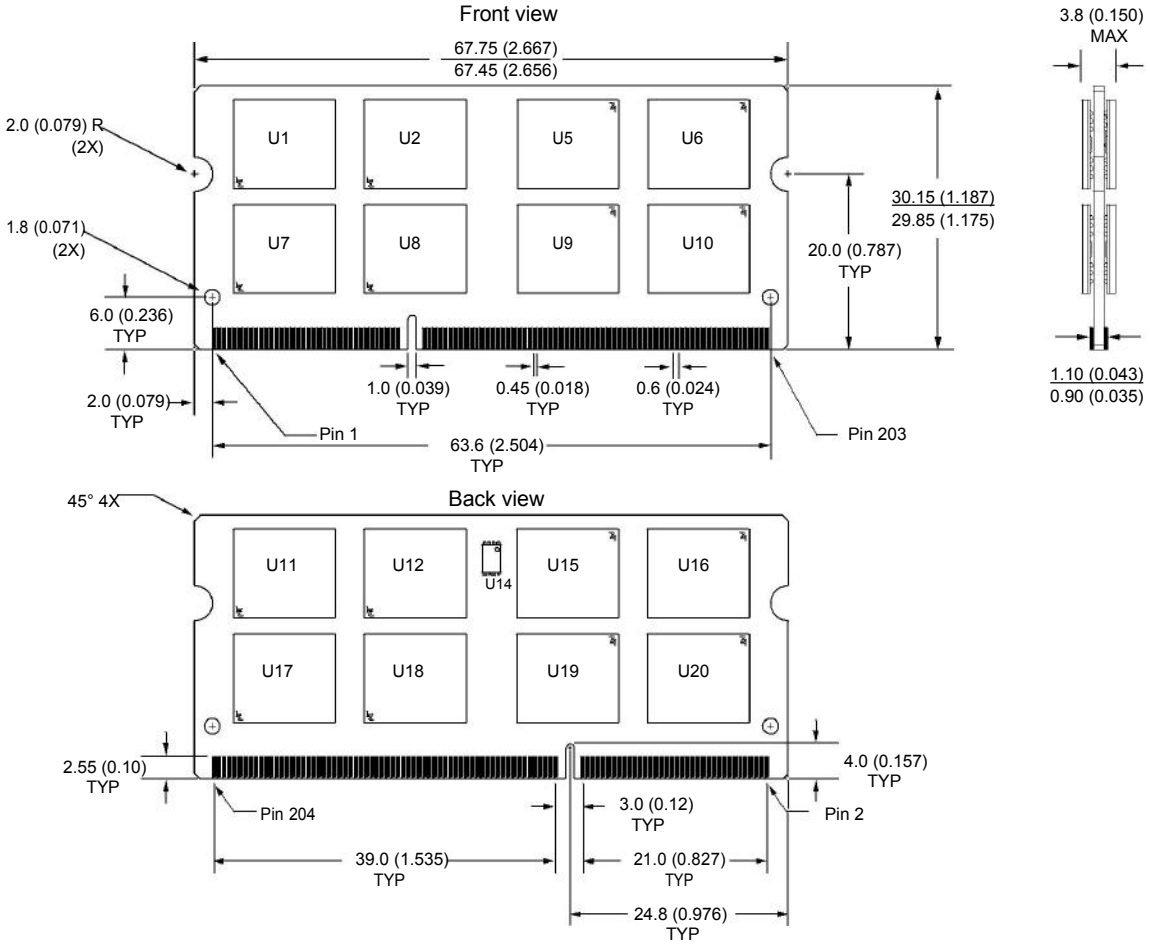
Table 19: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	t_{SCL}	10	400	kHz	
Clock pulse width HIGH time	t_{HIGH}	0.6	–	µs	
Clock pulse width LOW time	t_{LOW}	1.3	–	µs	
SDA rise time	t_R	–	300	µs	1
SDA fall time	t_F	20	300	ns	1
Data-in setup time	$t_{SU:DAT}$	100	–	ns	
Data-in hold time	$t_{HD:DI}$	0	–	µs	
Data-out hold time	$t_{HD:DAT}$	200	900	ns	
Data out access time from SCL LOW	$t_{AA:DAT}$	0.2	0.9	µs	2
Start condition setup time	$t_{SU:STA}$	0.6	–	µs	3
Start condition hold time	$t_{HD:STA}$	0.6	–	µs	
Stop condition setup time	$t_{SU:STO}$	0.6	–	µs	
Time the bus must be free before a new transition can start	t_{BUF}	1.3	–	µs	
WRITE time	t_W	–	10	ms	

Notes:
1. Guaranteed by design and characterization, not necessarily tested.
2. To avoid spurious start and stop conditions, a minimum delay is placed between the fall-ing edge of SCL and the falling or rising edge of SDA.
3. For a restart condition, or following a WRITE cycle.

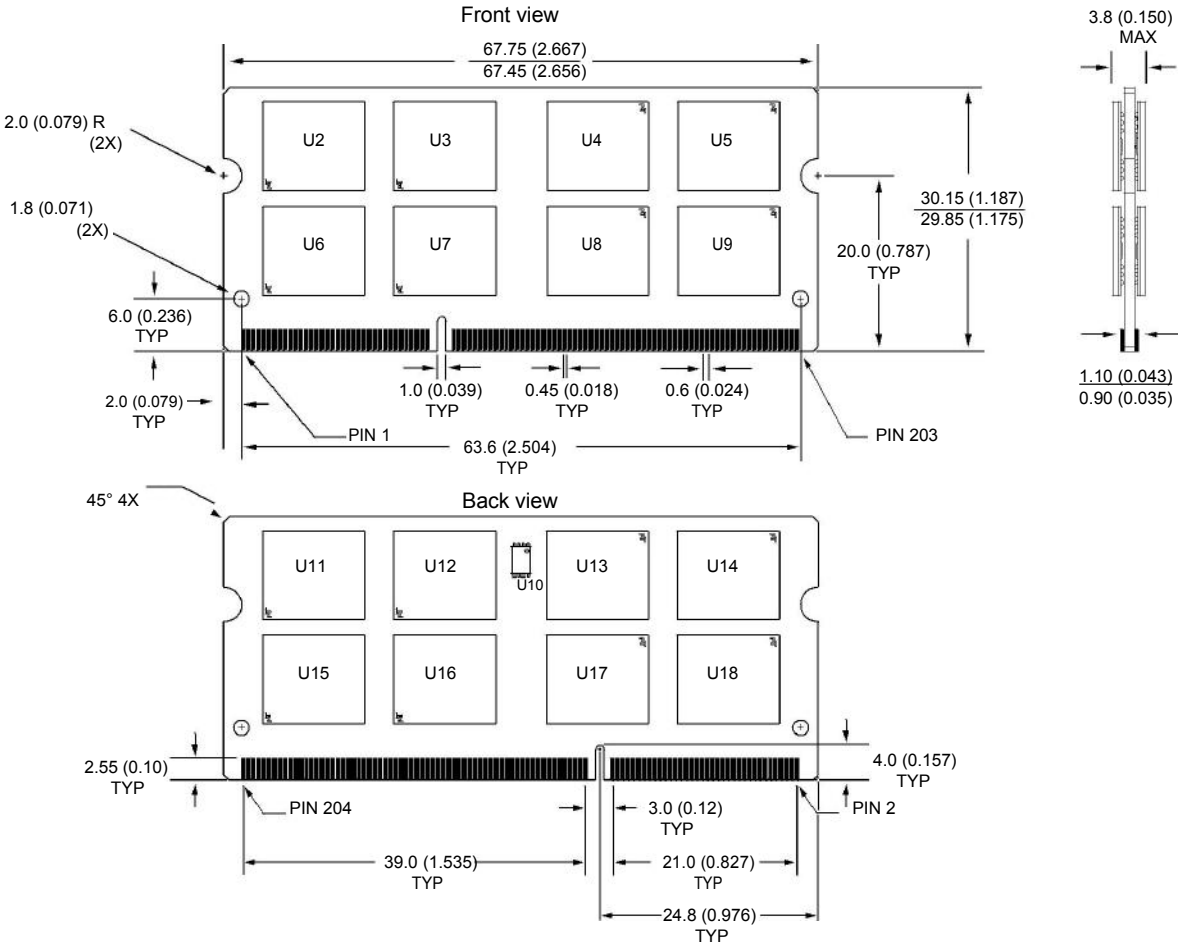
Module Dimensions

Figure 4: 204-Pin DDR3 SODIMM (PCB 0900, R/C-F)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted. 2. The dimensional diagram is for reference only.

Figure 5: 204-Pin DDR3 SODIMM (PCB 1569, R/C-F3)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted. 2. The dimensional diagram is for reference only.