DESCRIPTION

This document describes is 2048M x 64 one rank 8GB DDR4-2666 CL19 1.2v SDRAM unbuffered So-DIMM product.

The Micron DRAM is based on 8C 2048M x8-bit DDR4 FBGA components. The SPD is programmed follow JEDEC standard for 2666Mbps timing of 19-19-19 at 1.2v low power.

This product design specification reference JEDEC standard(*No. 21C DDR4 SDRAM SODIMM Design Specification*) raw-card A1.

This 260-pin So-DIMM uses gold contact fingers and requires +1.2v power supply .

This product's outline reference JEDEC design MO310.

Features

- VDD = VDDQ = 1.2V ±60mV
- VPP = 2.5V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 85°C
- 64ms, 8192-cycle refresh at 0°C to 85°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination(ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Post package repair (PPR) and soft post package repair (sPPR) modes
- JEDEC JESD-79-4 compliant

Addressing

Parameter	2048Meg x 8bit
Number of bank groups	4
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	32K (A[15:0])
Column addressing	1K (A[9:0])
Page size	1KB

Bank Group x8 Block Diagram
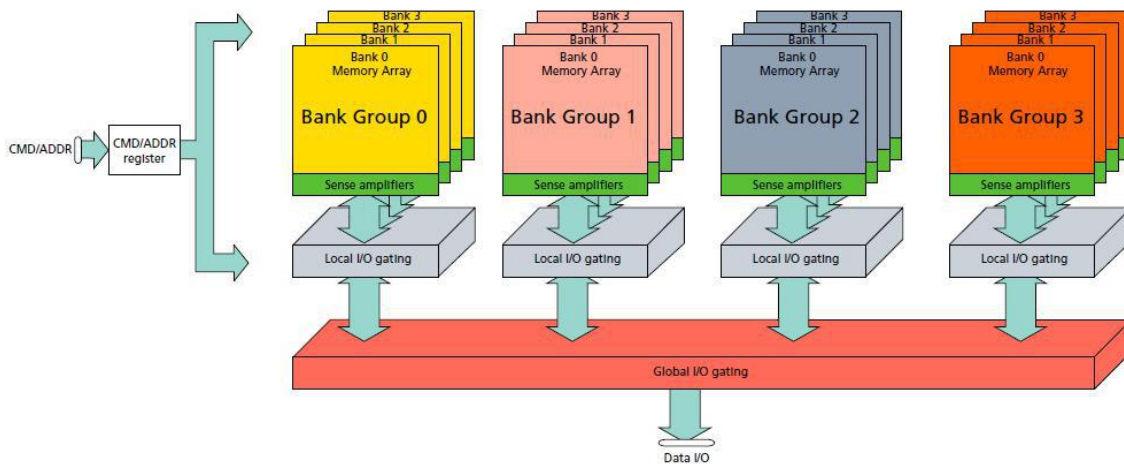
Ordering Information

Memory Type	Density	Organization	Component Composition	#of ranks
DDR4 NB 16G 2666	16GB	2048Mx64bit	2048M*8 8C	1

x8 Package Ball out (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

Pin Assignments

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	VSS	2	VSS	131	A3	132	A2
3	DQ5	4	DQ4	133	A1	134	EVENT_n
5	VSS	6	VSS	135	VDD	136	VDD
7	DQ1	8	DQ0	137	CK0_t	138	CK1_t
9	VSS	10	VSS	139	CK0_c	140	CK1_c
11	DQS0_c	12	DM0_n,DBI0_n,NC	141	VDD	142	VDD
13	DQS0_t	14	VSS	143	PARITY	144	A0
15	VSS	16	DQ6				
17	DQ7	18	VSS		**KEY**		
19	VSS	20	DQ2	145	BA1	146	A10/AP
21	DQ3	22	VSS	147	VDD	148	VDD
23	VSS	24	DQ12	149	CS0_n	150	BA0
25	DQ13	26	VSS	151	A14/WE_n	152	A16/RAS_n
27	VSS	28	DQ8	153	VDD	154	VDD
29	DQ9	30	VSS	155	ODT0	156	A15/CAS_n
31	VSS	32	DQS1_c	157	CS1_n	158	A13
33	DM1_n,DBI1_n,NC	34	DQS1_t	159	VDD	160	VDD
35	VSS	36	VSS	161	ODT1	162	C0,CS2_n,NC
37	DQ15	38	DQ14	163	VDD	164	VREFCA
39	VSS	40	VSS	165	C1,CS3_n,NC	166	SA2
41	DQ10	42	DQ11	167	VSS	168	VSS
43	VSS	44	VSS	169	DQ37	170	DQ36
45	DQ21	46	DQ20	171	VSS	172	VSS
47	VSS	48	VSS	173	DQ33	174	DQ32
49	DQ17	50	DQ16	175	VSS	176	VSS
51	VSS	52	VSS	177	DQS4_c	178	DM4_n,DBI4_n,NC
53	DQS2_c	54	DM2_n,DBI2_n,NC	179	DQS4_t	180	VSS
55	DQS2_t	56	VSS	181	VSS	182	DQ39
57	VSS	58	DQ22	183	DQ38	184	VSS
59	DQ23	60	VSS	185	VSS	186	DQ35
61	VSS	62	DQ18	187	DQ34	188	VSS
63	DQ19	64	VSS	189	VSS	190	DQ45
65	VSS	66	DQ28	191	DQ44	192	VSS
67	DQ29	68	VSS	193	VSS	194	DQ41
69	VSS	70	DQ24	195	DQ40	196	VSS
71	DQ25	72	VSS	197	VSS	198	DQS5_c
73	VSS	74	DQS3_c	199	DM5_n, DBI5_n,NC	200	DQS5_t
75	DM3_n,DBI3_n,NC	76	DQS3_t	201	VSS	202	VSS
77	VSS	78	VSS	203	DQ46	204	DQ47

#	Signal	#	Signal	#	Signal	#	Signal
79	DQ30	80	DQ31	205	VSS	206	VSS
81	VSS	82	VSS	207	DQ42	208	DQ43
83	DQ26	84	DQ27	209	VSS	210	VSS
85	VSS	86	VSS	211	DQ52	212	DQ53
87	CB5,NC	88	CB4,NC	213	VSS	214	VSS
89	VSS	90	VSS	215	DQ49	216	DQ48
91	CB1,NC	92	CB0,NC	217	VSS	218	VSS
93	VSS	94	VSS	219	DQS6_c	220	DM6_n,DBI6_n,NC
95	DQS8_c	96	DM8_n,DBI8_n,NC	221	DQS6_t	222	VSS
97	DQS8_t	98	VSS	223	VSS	224	DQ54
99	VSS	100	CB6,NC	225	DQ55	226	VSS
101	CB2,NC	102	VSS	227	VSS	228	DQ50
103	VSS	104	CB7,NC	229	DQ51	230	VSS
105	CB3,NC	106	VSS	231	VSS	232	DQ60
107	VSS	108	RESET_n	233	DQ61	234	VSS
109	CKE0	110	CKE1	235	VSS	236	DQ57
111	VDD	112	VDD	237	DQ56	238	VSS
113	BG1	114	ACT_n	239	VSS	240	DQS7_c
115	BG0	116	ALERT_n	241	DM7_n,DBI7_n,NC	242	DQS7_t
117	VDD	118	VDD	243	VSS	244	VSS
119	A12	120	A11	245	DQ62	246	DQ63
121	A9	122	A7	247	VSS	248	VSS
123	VDD	124	VDD	249	DQ58	250	DQ59
125	A8	126	A5	251	VSS	252	VSS
127	A6	128	A4	253	SCL	254	SDA
129	VDD	130	VDD	255	VDDSPD	256	SA0
				257	VPP	258	VTT
				259	VPP	260	SA1

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD/TS
RAS_n1	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n2	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n3	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)	VTT	mination supply for the Address, Com- mand and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1.RAS_n is a multiplexed function with A16.

2.CAS_n is a multiplexed function with A15.

3.WE_n is a multiplexed function with A14.

Input/Output Pin Functional Descriptions

Symbol	Type	Polarity	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Cross Point	Clock: CK_t and CK_care differential clock inputs. crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Active High	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit.After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence,they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Active Low	Chip Select: All commands are masked when CS_n is r selection on systems with multiple Ranks. CS_n is considered part of the command code. egistered HIGH. CS_n provides for external Rank
C0, C1	Input	High	Chip ID: Chip ID is only used for 3DS for 2 and 4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	Active High	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Active Low	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Active Low	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Active Low	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.

BG0 - BG1	Input	Active High	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components, only BG0 is valid.
BA0 - BA1	Input	Active High	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Active High	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n,RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Active High	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	---	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	---	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	---	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	---	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.
PARITY	Input	---	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15,WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW

ALERT_n	Output	Active Low	ALERT: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH.If there is error in Command Address Parity Check, then ALERT_n goes LOW for A relatively long period until on-going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input.Using this signal or not is dependent on the system.
SA0-SA1		---	Device address for the SPD.
RFU		---	Reserved for Future Use. No on-DIMM electrical connection is present.
NC		---	No Connect: No on-DIMM electrical connection is present.
VDD1	Supply	---	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	---	Ground
VTT2	Supply	---	Power Supply: 0.6 V
VPP	Supply	---	DRAM Activating Power Supply: 2.5 V (2.375 V min, 2.75 V max)
VREFCA	Supply	---	Reference voltage for CA
VDDSPD	Supply	---	Power supply used to power the I2C bus on the SPD.

Note:

1. For PC4, VDD 1.2V. For PC4L VDD is TBD.
2. For PC4, VTT is 0.6V. For PC4L VTT is TBD.

AC & DC Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃	1,2

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.3V~1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3V~1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3V~3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3V~1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	℃	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indi-cated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

DDR4-2666V Speed Bins

Speed Bin		DDR4-2666V		Unit
CL - nRCD - nRP		19-19-19		
Parameter	Symbol	min	max	
Internal read command to first data	t_{AA}	13.75	18.00	ns
Internal read command to first data with read DBI enabled	t_{AA_DBI}	tAA(min) + 3nCK	tAA(max) +3nCK	ns
ACT to internal read or write delay time	t_{RCD}	13.75	-	ns
PRE command period	t_{RP}	13.75	-	ns
ACT to PRE command period	t_{RAS}	32	9 x tREFI	ns
ACT to ACT or REF command period	t_{RC}	45.75	-	ns

PCB

- General
* Board size：69.6 x 30 mm   ±0.15 mm
* Thickness：1.2 ±0.1 mm
* Panel：6 pieces PCB per panel
* Impedance：50/55 Ohm ±10% (Single-ended)
                     57/70/83 Ohm ±15% (Differential)
* Pin count：260 PIN

- PCB Material
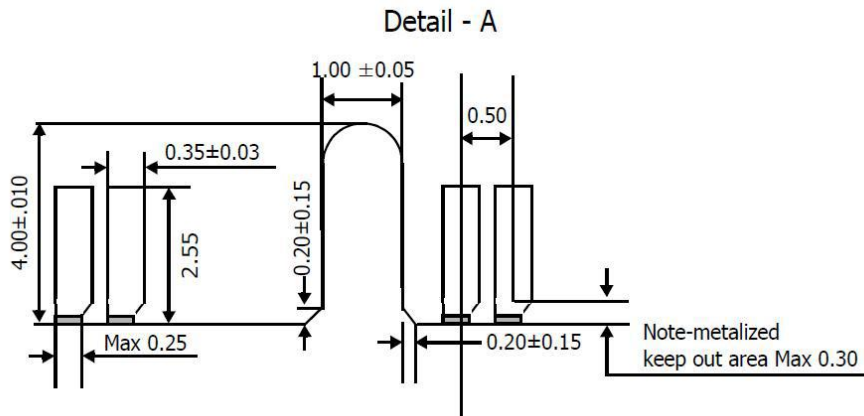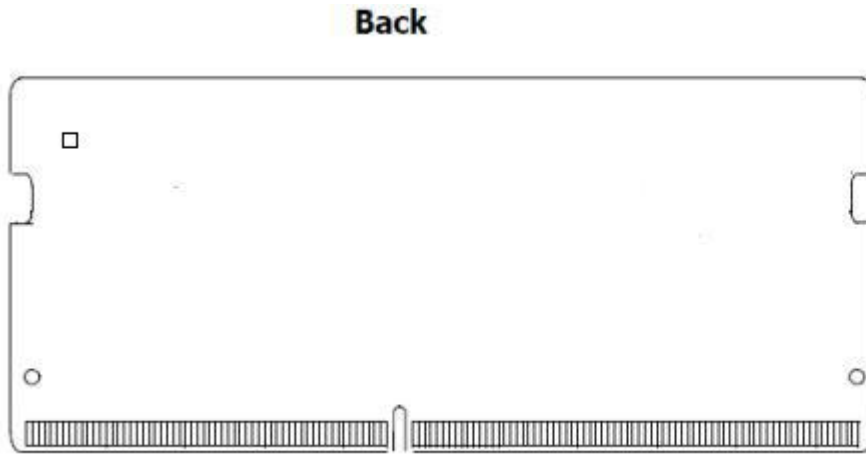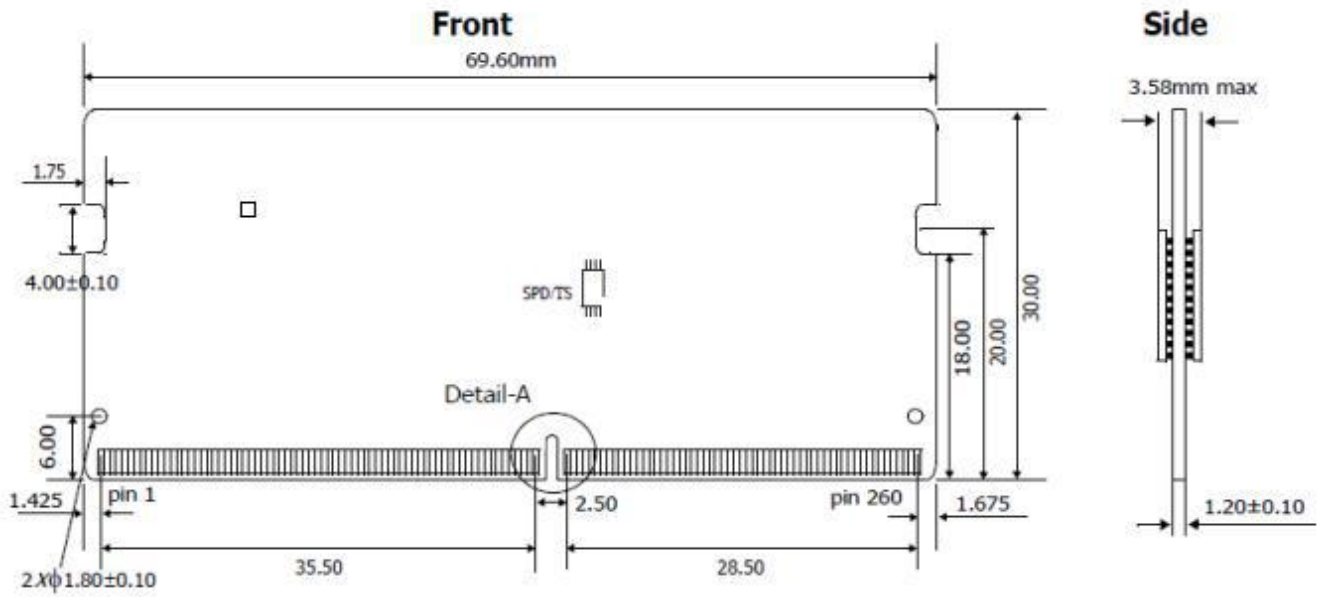* Glass Epoxy FR4 , .UL 94V-0, BP ML

- Plating
*Edge Connector Plating: Nickel Followed by gold
> Nickel Plating Thickness: 100 u" min.
> Surface treatment:
      Gold Plating: 3u" min.
      SMT PAD: average 2~3u".

- Reference:
*JEDEC Raw Card Version A1 200

Raw Card	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# of Banks in Inside DARM	# Address bits row/col
A1	16GB	2Gx64	16G bit	2048 M x 8	8	1	FBGA	16	16/10

![NTC RAM logo]

Module Dimensions

Front

69.60mm

1.75

4.00±0.10

6.00

1.425

pin 1

2.X φ1.80±0.10

35.50

Detail-A

2.50

pin 260

28.50

1.675

18.00

20.00

30.00

SPD/TS

Side

3.58mm max

1.20±0.10

Back

Detail - A

1.00 ±0.05

0.50

0.35±0.03

4.00±.010

2.55

0.20±0.15

Max 0.25

0.20±0.15

Note-metalized
keep out area Max 0.30

TOP SIDE 1-RANK WITHOUT ECC

B84SRCA1 HF 2.00

C1 C2 C3 C4

C9
C10

C11

R1

C12
C13
C14
C15
C16

U1 U2

R2

C17

C18

C19

C20

C5 C6 C7

C8
RN1
C34
RN2
C35
RN3
C36
RN4
C37

C21
C22

C23

R3

C24
C25
C26
C27
C28

U3 U4 U5

R4

C29

C30

C31

C32

C33

R5--------R26 C38 C39 C40 R27--------R48 C41

1

259

BOTTOM SIDE 1-RANK WITHOUT ECC

C42
RN5
C50
RN6
C51
RN7
C52
R49
R50
C53

C43 C44 C45

C54
C55
C56

U6 U7

R51

C57
C58
C59
C60

R52

C61

C62

C63

C64

C65

C46 C47 C48 C49

C66

C67

C68

R53

C69
C70
C71
C72

U8 U9

R54

C73
R55
C74

C75

C76

C77

C78 R56--------R77 C79 R78 R79 C80 C81 R80--------R101

260

2